Chapter 3

Nanoarchitecture of Quantum-Dot Cellular Automata (QCA) Using Small Area for Digital Circuits

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Additional information is available at the end of the chapter

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Abstract

Novel digital technologies always lead to high density and very low power consumption. One of these concepts—quantum-dot cellular automata (QCA), which is one of the new emerging nanotechnologies, is based on Coulomb repulsion. This chapter presents a novel design of 2-input Exclusive-NOR (XNOR)/Exclusive-OR (XOR) gates with 3-input Exclusive-NOR (XNOR) gates which are composed of 10 cells on 0.006 μm^2 of area. A novel architecture of 3-input Exclusive-OR (XOR) gate is defined by 12 cells on 0.008 μm^2 of area. The proposed design of 2-input XOR/XNOR gate structures provide less area and low complexity than the best reported design. The simulation results of proposed designs have been achieved using QCA Designer tool version 2.0.3.

Keywords: quantum-dot cellular automata (QCA), nanoelectronic, QCA technology, majority voter, Exclusive OR (XOR) gate, QCA Designer

1. Introduction

In recent years, the use of CMOS technology is limited by high consumption, low speed, and density beyond 10 nm. To overcome these problems, a number of researchers have been ascertained to find the solution for this classical CMOS technology which is quantum-dot cellular automata (QCA) used for high-speed application.

Nowadays, QCA transistor-less technology, single electron transistor (SET), and carbon nanotube (CNT) are being used as an alternative to CMOS technology. The use of QCA on the nanoscale has a promising future because of its ability to achieve high performance in terms of clock frequency, device density, and power consumption [1–4] if it is compared to similar implementations with conventional VLSI technology. These advantages make the proposed QCA technology useful for high-performance electronic applications applied on mobile or autonomous devices where power consumption and real-time processing low are needed.

Recently, using QCA technology for electronic modules design has become widely used [5–7]. In [8–10], memory circuits have been proposed. In [11–13], reversible full adder/subtractor and multiplier has been designed. In [14], a sequential circuits based on QCA technology has been proposed. In [15], a decoder circuit based on QCA technology has been developed.

In this chapter, we will describe the background of QCA technology. This new concept will take the great advantage of a physical effect called the Coulomb force. In the next, we will describe how the information can be propagated through QCA cell by clicking. Then, we will introduce the basic elements and gates used for QCA circuits. The proposed 2-input "XOR" circuit occupies small area of 0.006 μm^2, low complexity of 10 cells as compared to previous best designs. Besides, the proposed 3-input "XOR" design occupies only 0.008 μm^2 whereas the previous best reported design occupies 0.0116 μm^2 area. On the other hand, the proposed 3-input "XOR" gate has 32% less area than best reported design.

2. Background of QCA

In 1993, Craig Lent [16] proposed a new concept called quantum-dot cellular automata (QCA). This emerging technology has made a direct deviation to replace conventional CMOS technology based on silicon [17]. QCA generally uses arrays of coupled quantum dots in order to implement different Boolean logic functions. QCA or quantum-dot cellular automata as its name is pronounced uses the quantum mechanical phenomena for the physical implementation of cellular automata. In the general case, conventional digital technologies require a range of voltages or currents to have logical values, whereas in QCA technology, the position of the electrons gives an idea of the binary values [18]. The advantages of this technology are [19] especially given in terms of speed (range of terahertz), density (50 Gbits/cm^2) [20] and in terms of energy or power dissipation (100 W/cm^2).

QCA is based essentially on a cell. Each cell represents a bit by a suitable charge configuration as shown in **Figure 1**. It consists of four quantum dots and two electrons charge. Under the effect of the force of Colombian repulsion, the two electrons can be placed only in two quantum sites diametrically opposite.

A QCA cell is composed of four points with one electron each in two of the four points occupying diametrically opposite locations. The question that arises in this case is why do electrons occupy quantum dots of opposite or diagonal corner To answer this question, it is enough to have an idea about the principle of the repulsion of Coulomb, which is less effective with respect to the electrons when they are in adjacent quantum dots. The points are coupled to one another by tunnel junctions.

Thus, the internal effect of the cell highlights two configurations possible; each one will be used to represent a binary state "0" or "1." A topology of QCA is a paving of cells QCA. The interaction between the cells makes it possible to transmit information which gives the possibility of replacing physical interconnection of the devices. The information (logic 0 or logic 1) can propagate from input to the output of the QCA cell only by taking advantage of the force of repulsion as shown in **Figure 2**.

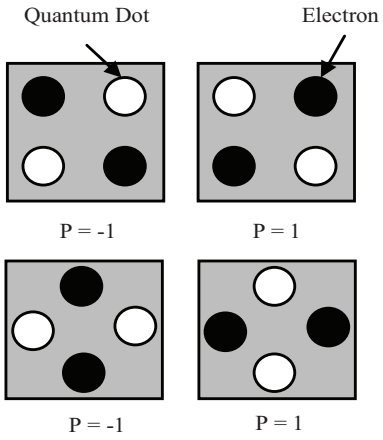


Figure 1. Basic QCA cell.

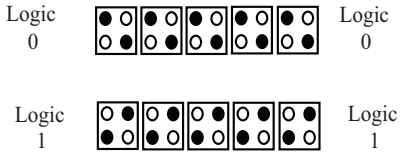


Figure 2. Operations of a QCA wire propagation by application of logic 0 and logic 1 1 to a QCA cell at the input.

3. Clocking in QCA

Clocking is an important term in QCA design. In order to propagate the information through QCA without any random adjustments of QCA cells, it is necessary to make a clock to guarantee the same data putting from input to the output. According to **Figure 3**, timing in QCA is obtained by clocking in four distinct periodic phases [21, 22] namely Switch, Release, Relax, and Hold.

Based on the position of the potential barrier, the arrays of QCA cells in each phase have different polarizations. There are four phases, and every phase has its own polarizations as shown in **Table 1**.

From **Table 1**, during the "Switch" phase of the clock, the QCA cell begins without polarization and switches to polarized state while the potential barrier has been raised from low to high. In the "'Hold" phase, the polarization state is preserved as the preceding phase and the potential barrier is high. From the "'Release" phase, the potential barrier is lowered and the cells become unpolarized. In "Relax" phase, the potential barrier remains lowered and the cells keep at nonpolarized state. This phase, the cells are ready to switch again. This way information is propagated in QCA circuits by keeping the ground-state polarization all the time. **Figure 4** illustrates the polarizations and interdot barriers of the QCA cells in each of the QCA clock zones.

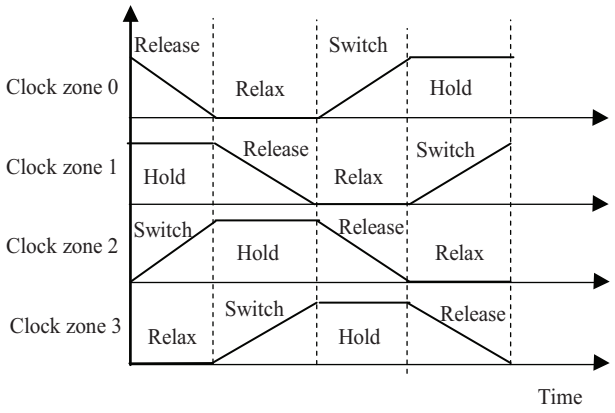


Figure 3. Four phases of QCA clock zones.

Clock phase	Potential barrier	Polarization state of the cells
Hold	Held high	Polarized
Switch	Low to high	Polarized
Relax	Low	Unpolarized
Release	Lowered	Unpolarized

Table 1. Operation of QCA clock phases.

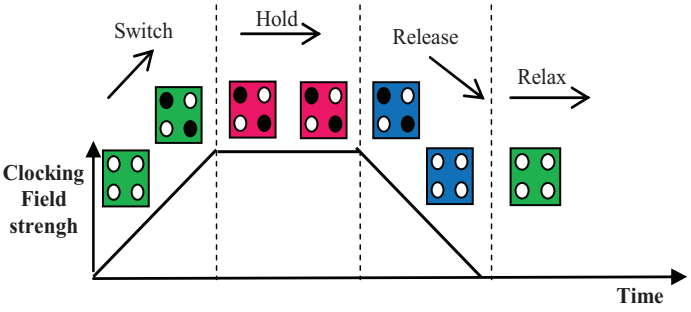


Figure 4. Schematic of interdot barriers in QCA clock.

4. Basic QCA elements and gates

Many architectures of logic devices can be designed by using adequate arranging of QCA cells. The biggest advantage of this wireless technology is that the logic is carried by the cells

themselves. The fundamental QCA logic is binary wire, inverter, and majority voter. These QCA logic gates are evaluated and simulated using the QCA Designer tool version 2.0.3.

4.1. Noninverter gate or binary wire

The great advantage of cell QCA is that all the close cells are aligned on a specific polarization, which depends on the input cell or the driver cell. Hence, by arranging the cells side-by-side according to the type "0" or "1" applied to the input cell, any logic can be transferred. Consequently, this gate can play the role of a wire or binary interconnection or noninverter gate as shown in **Figure 5(a)**. The layout of each cell given by binary wire is represented in **Figure 5(b)**.

The simulation results of the noninverter gate are presented in **Figure 5(c)**. One waveform with one frequency is applied to the input (In), one waveform for the first clock (Clk 0), and one waveform for the binary wire outputs (Out). From simulation results of binary wire given by **Figure 5(c)**, the expression from the output pulses of the noninverter gate can be deduced, which is given by Eq. (1):

$$Out = In \ . \overline{Clk\ 0} \tag{1}$$

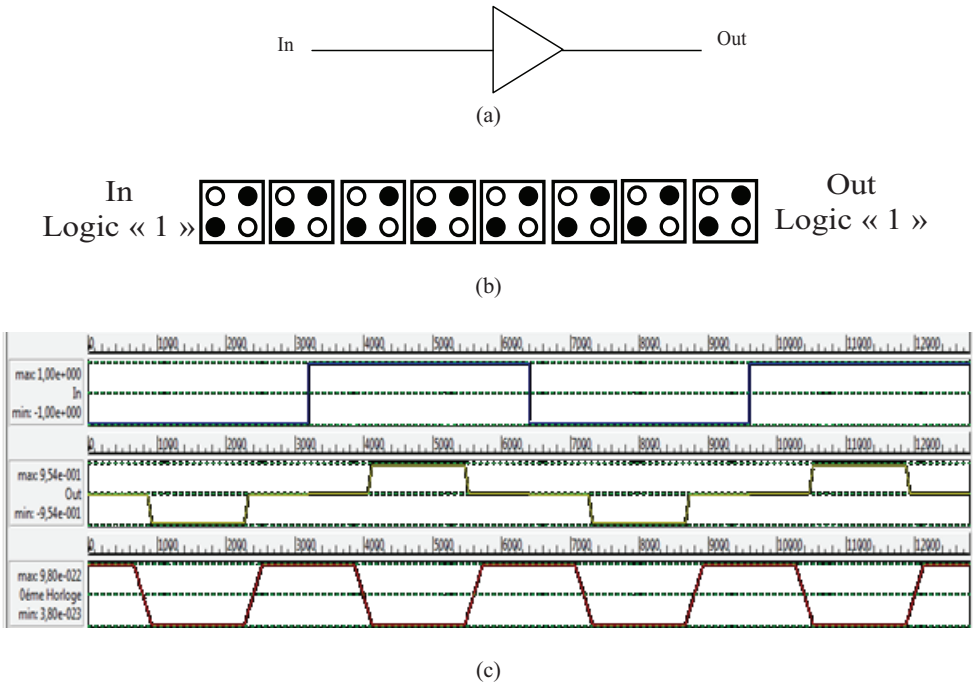


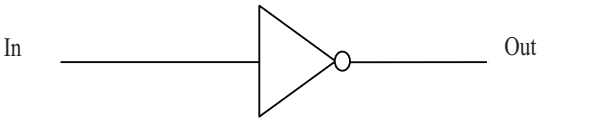
Figure 5. Binary wire, (a) representation, (b) QCA layout, and (c) simulation results.

4.2. Inverter gate

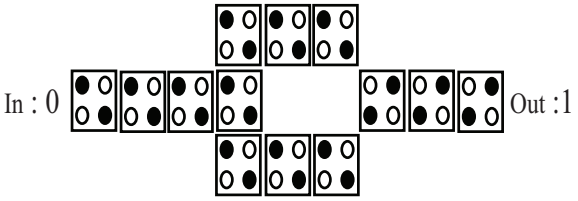
Thanks to the columbic interaction between electrons in neighboring cells, different types of the inverter gates in QCA were proposed [23–26]. The principle operation of this gate is to invert the input signal applied. If the applied input is low then the output becomes high and vice versa, as shown in **Figure 6(a)** and **6(b)**. The input "In" is given to one of the ends and the output reversed will be obtained at the output "Out." The position of the electrons and the layout of each cell are represented in **Figure 6(b)**. The principle of operation of this gate is based on the wire of input, which will be prolonged in two parallel wires and will polarize the cell placed at the end of these two wires, which implies the opposite polarization of this cell due to the Coulomb repulsion.

According to **Figure 6(c)**, the simulation results of the inverter gate are presented. One waveform with one frequency is applied to the input (In), one waveform for the clock 0 (Clk 0), and one waveform for the inverter gate outputs (Out).

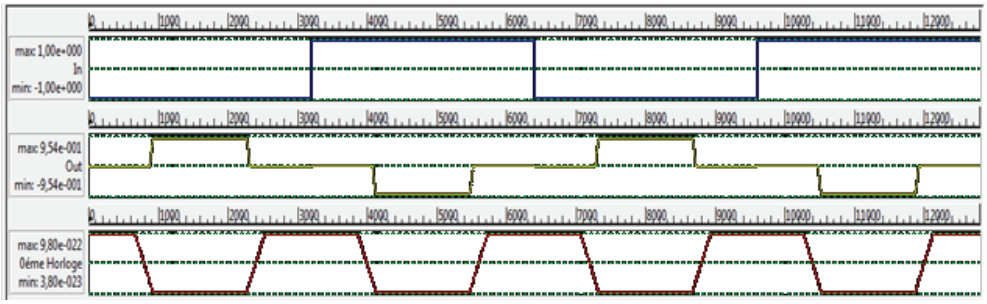
From simulation results of the output pulses inverter gate (Out) given by **Figure 6(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (2):



(a)



(b)



(c)

Figure 6. Inverter gate, (a) representation, (b) QCA layout, and (c) simulation results.

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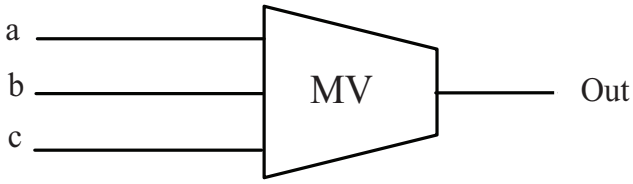
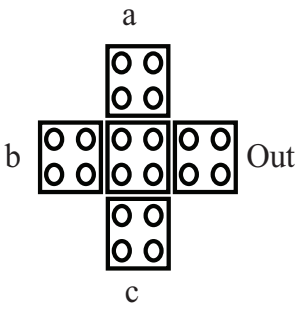
$$Out = \overline{In} \ . \overline{Clk}\ 0 \tag{2}$$

4.3. QCA majority voter

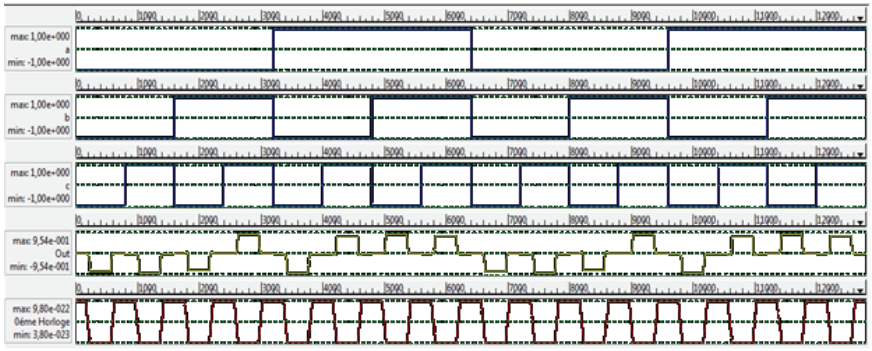
In QCA circuits, the majority voter (MV) plays an important role for logic gates. It is only composed of five cells: three input cell, one output cell, and a center cell, which is the decision-making cell. These cells are arranged like a cross with three inputs (a, b, and c) and one output (Out). This gate is based on the majority logic value given at its input as shown in **Figure 7(a)**. The layout of each cell given by MV is represented in **Figure 7(b)**.



(a)



(b)



(c)

Figure 7. Majority voter (MV) gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

According to **Figure 7(c)**, the simulation results of the majority voter (MV) gate are presented. Three waveforms with different frequencies are applied to the inputs (a, b, and c), one waveform for the clock 0 (Clk 0), and one waveform for the MV outputs (Out). From simulation results of the output pulses of MV gate given by **Figure 7(c)**, the expression of the MV gate can be given by Eq. (3):

$$Out = a \,.\, b + b \,.\, c + c \,.\, a \tag{3}$$

From the majority voter gate, depending on the input fixed to 0 or 1, other logical gates can be deduced such as AND/OR gates.

- On the one hand, when one of the inputs of MV is fixed to 1, the logical function of OR gate is obtained and can be expressed in Eq. (4):

$$Out = a + b \quad when \quad c = 1 \tag{4}$$

Figure 8 shows the representation, QCA layout, and simulation of OR gate.

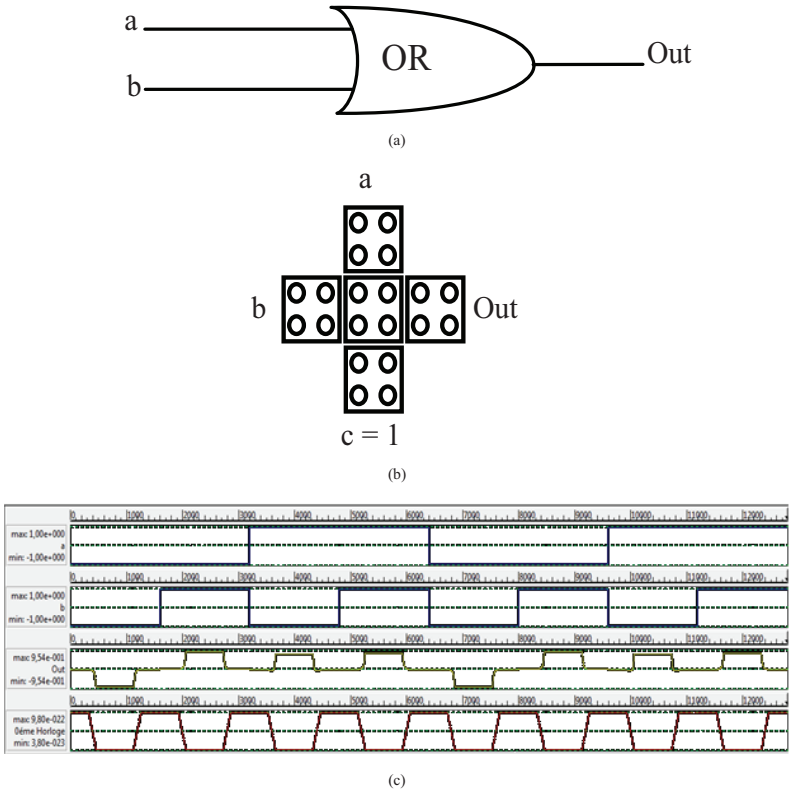


Figure 8. OR gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

According to **Figure 8(c)**, the simulation results of the OR gate are presented. Two waveforms with one frequency are applied to the inputs (a and b), one waveform for the clock 0 (Clk 0), and one waveform for the OR gate outputs (Out).

From simulation results of the output pulses OR gate (yellow) given by **Figure 8(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (5):

$$Out = (a + b).\overline{Clk}\ 0 \tag{5}$$

- On the other hand, when one of the inputs of MV is fixed to 0, the logical function of AND gate is obtained (**Figure 9**) and can be expressed in Eq. (6):

$$Out = a\ .\ b \quad when \quad c = 0 \tag{6}$$

Figure 9 shows the representation, QCA layout, and simulation of AND gate.

According to **Figure 9(c)**, the simulation results of the AND gate are presented. When there are two waveforms, with one frequency is applied to the inputs (a and b), one waveform given for the clock 0 (Clk 0), and one waveform for the AND gate outputs (Out).

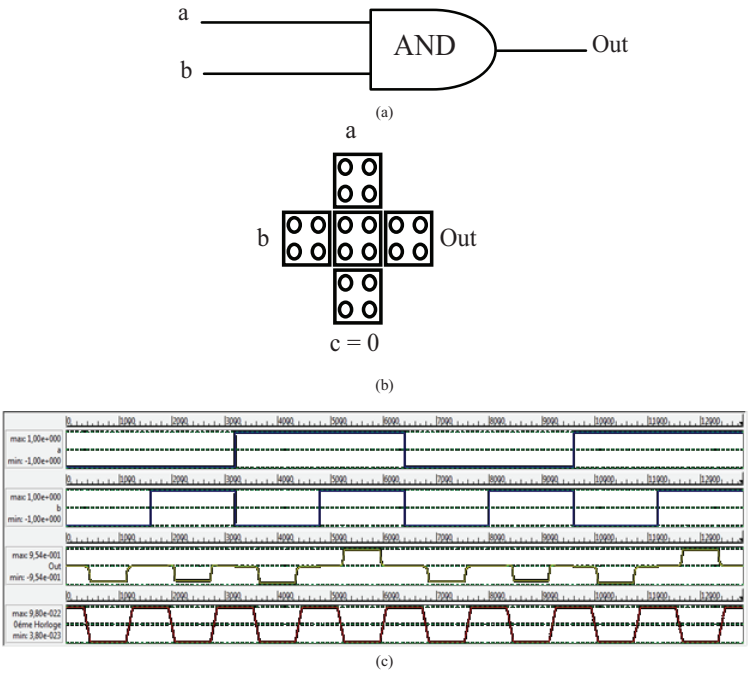


Figure 9. AND gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

From simulation results of the output pulses AND gate (yellow) given by **Figure 9(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (7):

$$Out = \quad (a \;.\; b).\overline{Clk}\;0 \tag{7}$$

5. Novel proposed QCA elements and gates

5.1. Proposed structure of 2-input digital "XNOR" gate

The 2-input logical "XNOR" gate is a hybrid circuit based on Inverter gate and "Exclusive-OR" gate. The schematic of a simple digital "XNOR" gate is presented in **Figure 10**. This circuit has two inputs: "c" and "d," and one output "K."

The truth table of this "XNOR" gate is shown in **Table 2**.

From **Table 2**, it can be deduced that when "c" and "d" are equal, the output "K" is equal to "1," and when "c" and "d" are different, the output "K" is equal to "0." Hence, the output "K" of the "Non-Exclusive-OR" ("XNOR") gate performs the following logic operation in Eq. (8):

$$K = \overline{c \oplus d} = \quad \overline{\overline{c}.d + c.\overline{d}} \tag{8}$$

In this chapter, a novel architecture of two-input "non-Exclusive-OR" gate using QCA implementation is proposed. It is defined by a higher density and a small number of cells.

This novel structure of 2-input "XNOR" gate is composed of two inputs "c," "d," and one fixed logic "0," with one output "K." The structure and the QCA layout of the proposed design are shown in **Figure 11**.

The simulation results of the proposed 2-input logical "XNOR" gate are shown in **Figure 12**. Four waveforms are applied to the inputs: c, d, Clk 0 and Clk 1. One waveform for the digital "XNOR" gate outputs (K). It can be deduced that there is 0.5 clock delay of latency on the novel proposed 2-input "XNOR" gate constituted only by 10 cells with an area of 0.006 μm^2.

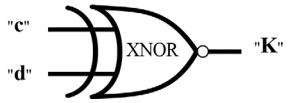


Figure 10. Schematic of 2-input "XNOR" gate.

c	d	K
0	0	1
0	1	0
1	0	0
1	1	1

Table 2. Truth table of 2-input "XNOR" gate.

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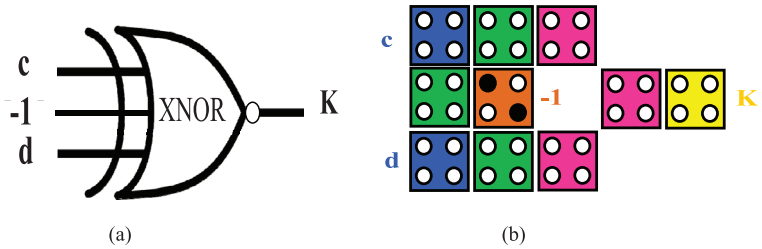

Figure 11. The novel architecture of 2-input "XNOR" gate structure, (a) schematic of "XNOR" gate and (b) QCA layout of proposed "XNOR" gate.

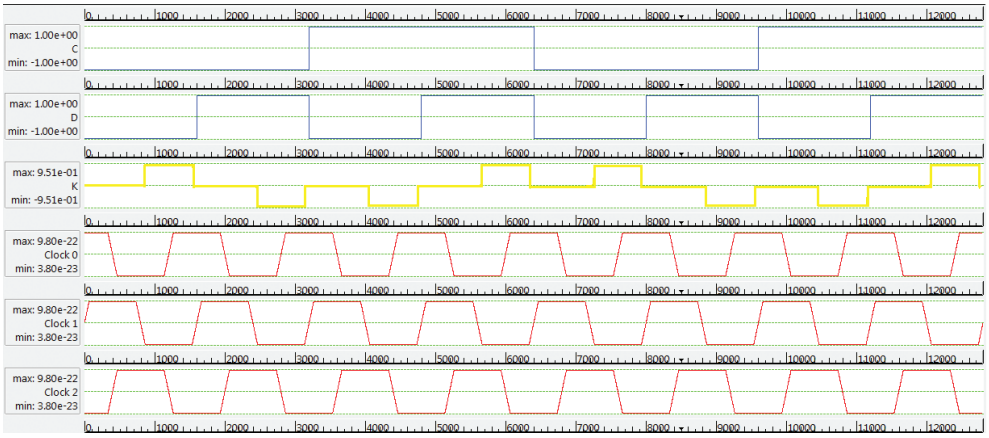

Figure 12. The simulation result of the novel design of 2-input logical "XNOR" gate.

5.2. Proposed structure of 3-input digital "XNOR" gate

The 3-input logical "XNOR" gate is adapted of 2-input logical "XNOR" gate. The schematic of this digital "XNOR" gate is presented in **Figure 13**. This circuit has four inputs: "c," "d," "e," and one output "K."

The truth table of this 3-input "non-Exclusive-OR" gate is shown in **Table 3**.

From **Table 3**, it can be deduced that when the number of the input "1" is odd, the output "K" is equal to "0." In the case of the number of the input "1" is even, the output "K" is equal to "1." Hence, the output "K" of the XNOR gate can determine the parity and is given by the following logic operation in Eq. (9):

$$K = \overline{c \oplus \quad d \oplus e} \tag{9}$$

The simulation results of the proposed 3-input logical "XNOR" gate are shown in **Figure 14**. Three waveforms are applied to the inputs (c, d, and e) with the clock 0, clock 1, and one

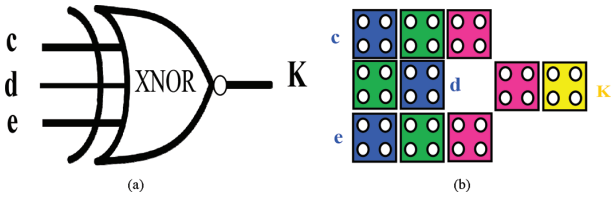

Figure 13. Schematic of 3-input "XNOR" gate. (a) Schematic of "XNOR" gate and (b) QCA layout of proposed "XNOR" gate.

c	d	e	k
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	

Table 3. Truth table of 3-input "XNOR" gate.

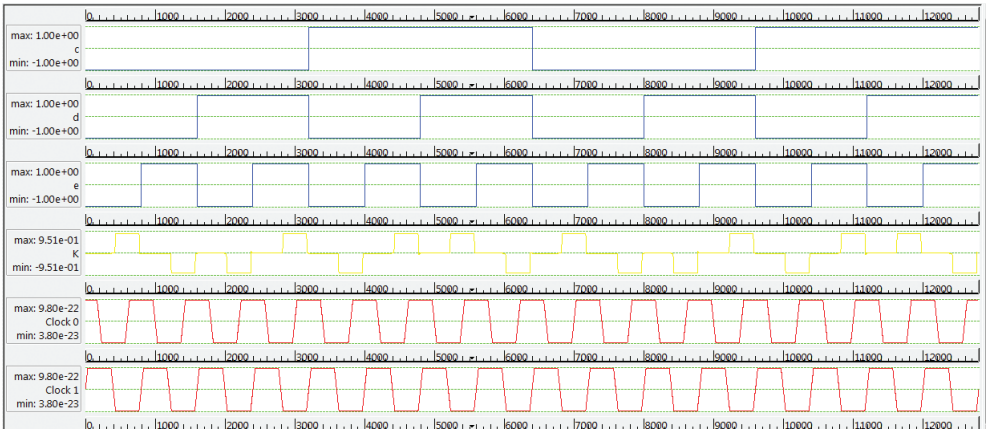

Figure 14. The simulation result of the novel architecture of 3-input logical "XNOR" gate.

waveform for the digital 3-input "XNOR" gate outputs (K). It can be deduced that there is 0.5 clock of latency on this novel proposed architecture 3-input "XNOR" gate constituted by 10 cells and with an area of 0.006 μm^2.

5.3. Proposed architecture of 2-input "XOR" gate

The 2-input logical "XOR" gate is a hybrid circuit, which is designed from 2-input logical "XNOR" gate. The schematic of "XOR" gate is presented in **Figure 15**. This circuit has two inputs: "c" and "d," and one output "K."

The truth table of this 2-input "Exclusive-OR" gate is shown in **Table 4**.

From **Table 4**, it can be deduced that when "c" and "d" are different, the output "K" is equal to "1," and when "c" and "d" are equal, the output "K" is equal to "0." Hence, the output "K" of the "Exclusive-OR" ("XOR") gate performs the following logic operation in Eq. (10):

$$K = c \oplus d = \bar{c} \,.\, d + c \,.\, \bar{d} \tag{10}$$

This novel design of 2-input "XOR" gate is composed of two inputs "c" and "d," and one fixed logic "0," with one output "K." The structure and the QCA layout of the proposed 2-input "XOR" gate are shown in **Figure 16**.

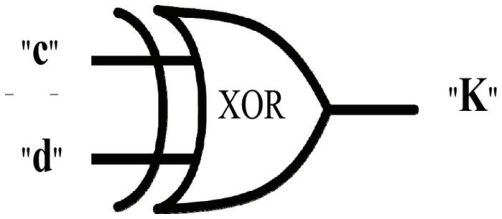

Figure 15. Schematic of 2-input "XOR" gate.

c	d	K
0	0	0
0	1	1
1	0	1
1	1	0

Table 4. Truth table of 2-input "XOR" gate.

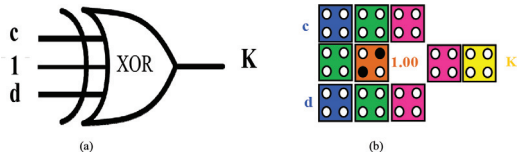

Figure 16. The architecture of novel design 2-input "XOR" gate structures: (a) schematic of 2-input "XOR" gate and (b) QCA layout of proposed 2-input "XOR" gate.

The simulation results of the proposed architecture of 2-input "XOR" gate are presented in **Figure 17**. Two waveforms are applied to the inputs (c and d), the clock 0, clock 1 and one waveform for "XOR" gate output (K). From **Figure 11**, it can be deduced that there is 0.5 clock of latency on this novel 2-input "XOR" gate, which is constituted by 10 cells with an area of 0.006 μm^2.

The proposed 2-input XOR circuit has lower computational complexity and better performances compared to the existing ones [27–31]. **Table 5** shows the comparison results of the proposed design for the XOR with the existing designs.

5.4. Proposed structure of 3-input "XOR" gate

The 3-input logical "XOR" gate is an adapted form of 3-input logical "XNOR" gate. The schematic of this digital "XOR" gate is presented in **Figure 18**. This circuit has only four inputs: "c," "d," "e," and one output "K."

The truth table of this 3-input "Exclusive-OR" gate is shown in **Table 6**.

From **Table 6**, it can be deduced that when the number of the input "1" is even, the output "K" is equal to "0". When the number of the input "1" is odd, the output "K" is equal to "1." Hence, the output "K" of the XNOR gate can determine the parity and is given by the following logic operation in Eq. (11):

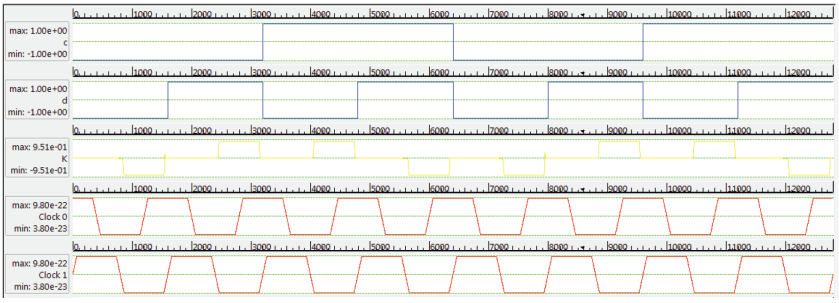

Figure 17. The simulation result of the novel structure of 2-input "XOR" gate.

Design	Cell count	Area (μm^2)	Latency
2-input XOR gate [27]	67	0.06	1.25
2-input XOR gate [28]	32	0.02	1
2-input XOR gate [29]	28	0.02	0.75
2-input XOR gate [30]	30	0.0233	0.75
2-input XOR gate [31]	12	0.0116	0.5
Proposed 2-input XOR	12	0.006	0.5

Table 5. Comparison results of single layer 2-input XOR gates.

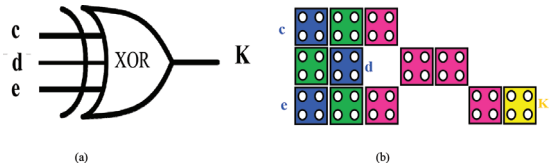

Figure 18. The architecture of novel design 2-input "XOR" gate structures: (a) schematic of 2-input "XOR" gate and (b) QCA layout of proposed 2-input "XOR" gate.

c	d	e	k
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 6. Truth table of 3-input "XOR" gate.

$$K = c \oplus \quad d \oplus e \tag{11}$$

The simulation results of the proposed 3-input logical "XOR" gate are shown in **Figure 19**. Three different waveforms are applied to the inputs (c, d, and e), the clock 0 and clock 1 and one waveform for the digital 3-input "XNOR" gate outputs (K). It can be interpreted that there

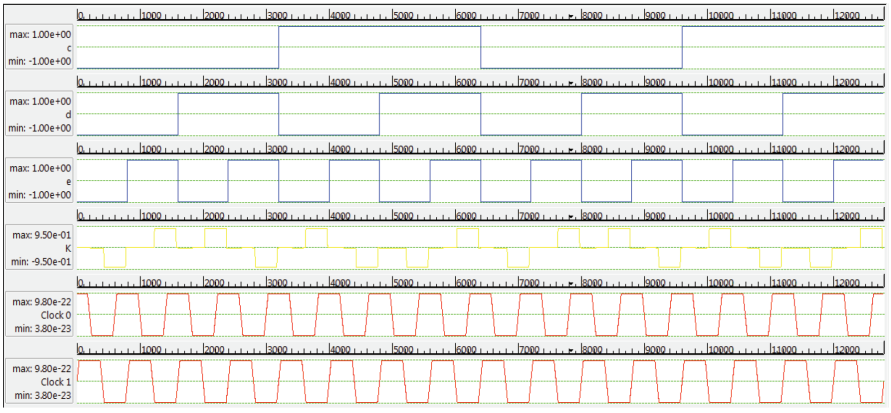

Figure 19. The simulation result of the novel architecture of 3-input "XOR" gate.

Design	Cell count	Area (μm^2)	Latency
3-input XOR gate [31]	12	0.0116	0.5
3-input XOR gate [27]	93	0.07	11.25
Proposed 3-input XOR gate	12	0.008	0.5

Table 7. Comparison results of single layer 3-input XOR gates.

is 0.5 clock of latency on this novel proposed structure of 3-input "XOR" gate, which is composed of 12 cells with an area of 0.008 μm^2.

Table 7 shows the comparison results of the proposed design for the 3-input XOR with the exist designs.

6. Conclusion

In this chapter, we have presented a QCA implementation of several fundamental basic elements and logic gates. Architectures and simulation results are also proposed. An important step in designing QCA circuits is reducing the number of required cells. The proposed method for the reduction of the number of cells in the QCA structure is based on the position of the electrons and the interaction forces between them. In the current proposed work, we have optimized the number of QCA cellule and reduced the wire crossings. Furthermore, this work may be extended to design other reversible QCA gates.

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