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Design of Sequential Circuit Using Quantum-Dot Cellular Automata (QCA)

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Abstract— *Quantum dot cellular autometa presents a promissing nanoscale technology for replacement of conventional cmos based circuits.In this paper we introduce qca logic gates such has qca inverter and qca majority gate.This paper design the sequential logic gates.such as D latch,SR latch,JK latch,T flipflop,D flipflop,2 bit counter,4 bit shift register.These designs are captured and simulated using a design calld QCA designer.*

Keywords— QCA,sequential circuits,QCADesigner.

I. INTRODUCTION

The performance and density of IC technology is increasing successfully with CMOS devices for fast few decades. To fabricate CMOS transistors into smaller and smaller size[1].It will eventually hits its limitations. Hence several alternatives have been proposed. QCA seems to suitable novel computing technology to replace the conventional CMOS technology.[2]

QCA technology was proposed by Criag S.Lent et al, in 1993[3]. The QCA paradigm in light of quantum dots which is more reasonable for logic circuits with superior and low power scattering at nanometer scale . In late year QCA innovation picked up part of prominence because of the enthusiasm for making registering devices and logic function implementation.

The main advantages of QCA technology

- high thickness
- very high operational recurrence
- low power utilization

In this paper D flip flop, gated D flip flop ,T flip flop, SR active high flip flop, SR active low flip flop, JK flip flop, 2 bit counter, 4 bit shift register are designed and simulated. in section II the basics of QCA is introduced .in section III methodology of flip flops and latches, counters and shift registers are introduced. In section IV simulation results of flip flops and latches, counters and shift registers are introduced.

II. QCA BACKGROUND

In this section we introduced QCA cells, QCA wires, QCA gates and QCA clocking zones.

a) QCA CELL

QCA circuits comprise of QCA cells. Each QCA cell can be considered as a square and four “dots”. These are placed at corners and each QCA cell has two electrons[4] .These two electrons occupy two diagonal quantum dots in the cell keeping maximum distance due to columbic repulsion each other. electrons in one diagonal position can change to each other diagonal position and these two directions are two polarizations. if electrons are present as shown in figure 1(b) polarization-1 which represent binary “0”.and if electron are shown in figure 1 (c) polarization is +1 which represent binary ‘1’[5].

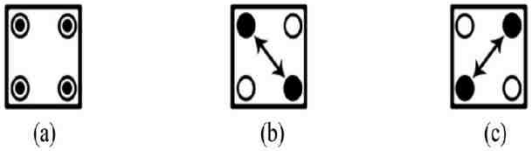


Fig.1: QCA cell a) Empty cell b) Polarization -1 c) Polarization+1

b) QCA WIRES

Wire in QCA is constructed by arranging some cells in a line. The binary information transmitted from one end to another end binary “1” or “0” which enters at first cell reach the last cell which depicted by figure 2(a) and 2(b) QCA wires are two types a)binary wire b)inverter chain.

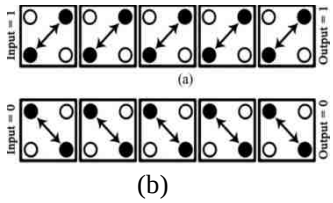


Fig.2: (a) Transmitting binary 1 (b) Transmitting binary 0

All cell in binary wire have the same polarization .the cells polarization in an inverter chain is changed alternatively.

c) QCA GATES

Like conventional logic circuits in which AND, OR, NOT gates are the basics gates, the basic logical gates in QCA are majority voter and NOT gates.

i) QCA INVERTER

When two pairs shifted horizontally or vertically becomes

orthogonal and complements from one pair to other pair. For example an input logic '1"is shown to be inverted in fig 3(a) a robust QCA inverter with seven cells has been designed in fig 3(b)[6].

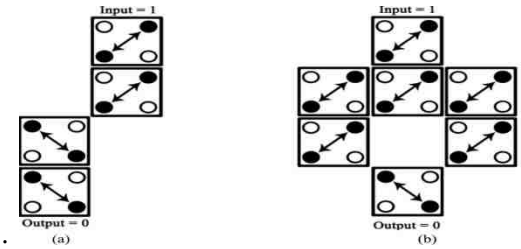


Fig.3: (a) Corner inverter (b) Robust inverter

ii) QCA MAJORITY VOTER

Majority voter is an important element in the QCA circuits MV is 3 input majority gate which consist of five cells in that 3 is inputs ,one is output and another one is center cell is evaluating cell. Center cell find the majority of binary information from 3 inputs and transmit to the output cell. A,B,C are input variables, Majority Voter expression is given by

$$Y = M(A,B,C) = AB + BC + CA \qquad (1)$$

If any one of the inputs of Majority Voter is assigned to '0', it will be equivalent to an AND gate. A OR gate can be achieved when one of the MV inputs is set to '1'. Majority Voter shown in the figure 4(a) and 4(b)

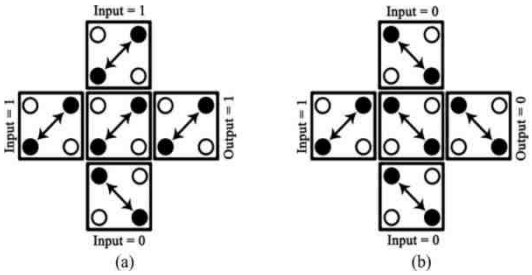


Fig.4 .Majority gates 1 and 0

iii) QCA CLOCKING

There are four clock phases to QCA cells: Switch phase, Hold phase, Release phase and Relax phase as depicted in figure5.[7], in the clock. Switch phase initially QCA cells are unpolarized and the potential barriers are low and they are polarize in switch phase and their barriers become high; computation occurs in this phase .in hold phase of the clock barriers remain at high. During the clock release phase, barriers go low and QCA cells remain at un polarized [8],[9],[10]. When clock is on the ground state interacts with excited states.

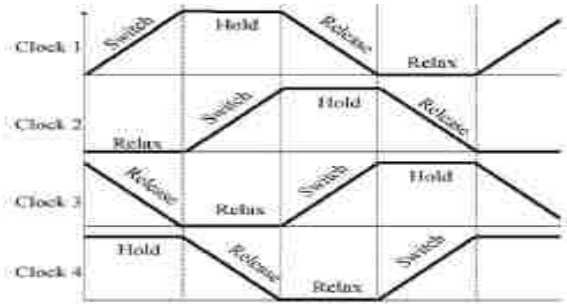


Fig.5: Clock phases in QCA

Clock zone based wire crossover : There are four clock zones in QCA cells and they are clock 0 (green), clock 1 (pink), clock 2 (cyan) and clock 3 (white) is depicted in figure 6.

Fig.6.QCA cell four clock zones

Each clock zone defers by 90^0 degrees, with its adjacent or next clock zone and clock 0, clock3 are adjacent to each other the inter section of two QCA wires can be implemented using 180^0 out of phase cells in two wires 1 so clock 0 and clock 2 can intersects to make a wire cross or clock 1 and clock 3 can intersect to make a wire cross, two wire clock zone based wire cross and their signal transmission are depicted in figure 7(a) and 7(b) respectively.

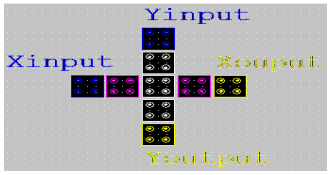


Fig.7:(a) clock 0,clock 2 clock zone cross over

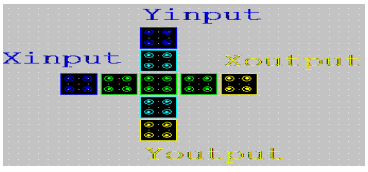


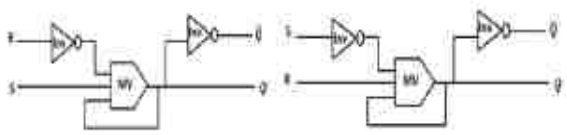
Fig.7:(b) .Clock 1 and clock 3 cross over

III. METHODOLOGY

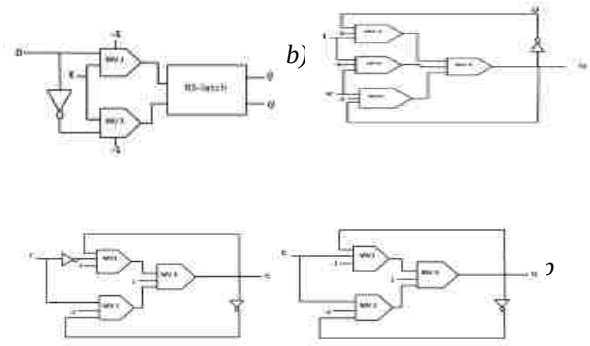
A) Flip flops and Latches

To design sequential circuits, the conventional CMOS circuits are not suitable to direct translated into QCA architecture due to timing constraint of the sequen logic circuits. Therefore, the truth tables of each sequential circuit have been observed and the Boolean equations have been derived for each circuit. From the relationship

of each variable can be clearly observed and number of required logic gates can be determined. Figure. 8 shows



the block diagrams of the presented latches and flip-flops presented.



d) T flip flop *f) D flip flop*

Fig.8. QCA block diagrams of latches and flip flops

B) Counters and Registers

Two major applications of latches and flip flops are registers and counters. From previous design work of Kong[11] and Janulis [12], a 4 bit synchronous binary up counter and 4 bit shift register are presented here. Fig 9.and 10 shows the block diagram of the two circuits.

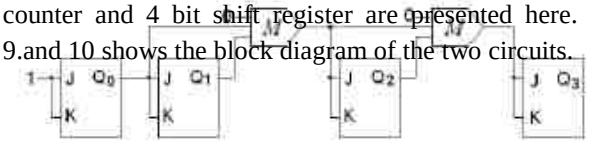


Fig. 9. Block diagram of 4 bit synchronous up counter

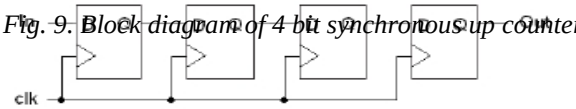


Fig. 10. Block diagram of 4-bit counter

IV. SIMULATION RESULTS

i) Latches and Flip Flops

The operation of D-latch is that its output will always follow its input. Figure 11(b) shows the simulation result of the chain by using QCA designer. It shows that the output always follwing the inputs by one clock cycle lagging. One clock cycle is a full set of clock assignment from clock 0 to clock 3 (four clock zones).

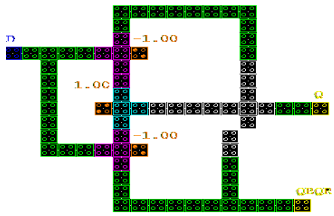


Fig. 11 (a) QCA D latch

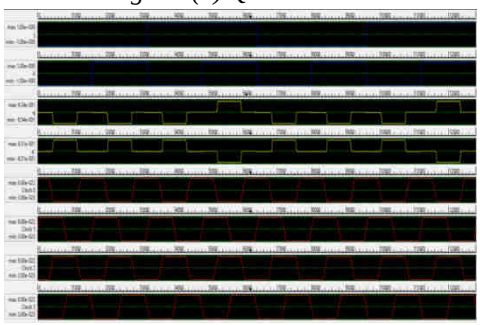


Fig. 11 (b) Simulation result of QCA D latch

Figure 12 shows the QCA RS latch proposed in [13] together with simulation results. For active high RS latch, the outputs SET when S=1 and R=0, outpput is RESET when R=1 and S=0. Contrary, the active low RS latch is the inverse of the active high RS latch. Their results are lagging of two clock cycles because of the clocking in the circuits. Both circuits use eight clock zones from input to output. Therefore, the circuit has a total of two clock cycles lagging for the outputs. The assignment of clock zones in the circuit is crucial in designing the sequential logic circuit to control the signal flow and synchronize the inputs entering the functional gate and the output. In this design, the inner loop is lagged of one clock cycle while the output is lagged of two clock cycles. It is important to assign the same clock zoned for the inputs of the majority gate to ensure the signal entering the gate is at the same time. In this case, two of the inputs of the majority gate are from the inputs S and R, which have the lagging of one clock cycle, and one of the Majority gate is only available after two clock cycles which is the same timing of the output so every output will then interact with the new inputs to generate the new output.

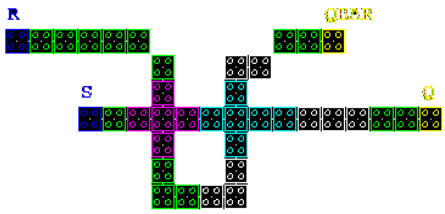


Fig. 12(a) QCA SR high latch

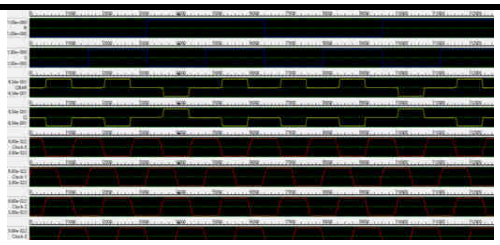


Fig. 12(b)simulation result of QCA SR active high latch

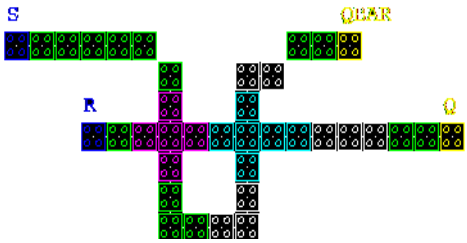


Fig. 12(a) QCA SR active low latch

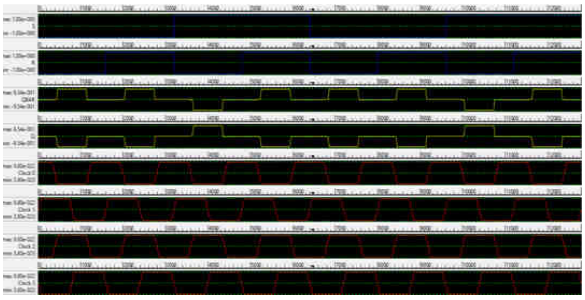


Fig. 12(b) QCA SR active low latch simulation result

Fig.13 shows the QCA design and simulation of gated D-latch .the gated D-latch only can function as D-latch when the enable bit is at logic 1.

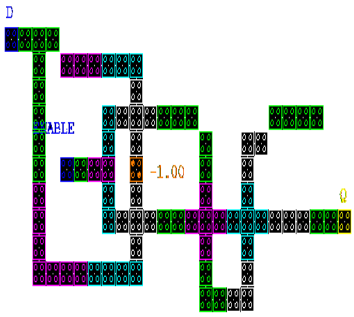


Fig.13(a) Gated D latch

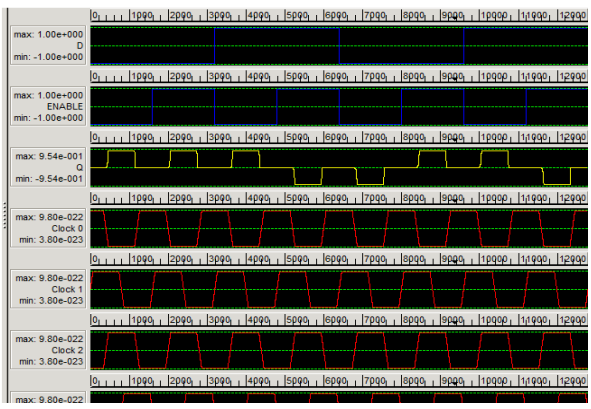


Fig. 13(b) Simulation result of gated D latch

Fig.14 shows the circuits of JK flip flop and its simulation using QCA Designer. JK flip flop has the ability to toggle the previous output when both of its inputs are logic 1.Other combinations of input J and input Kwill produce the same result as a RS latch.

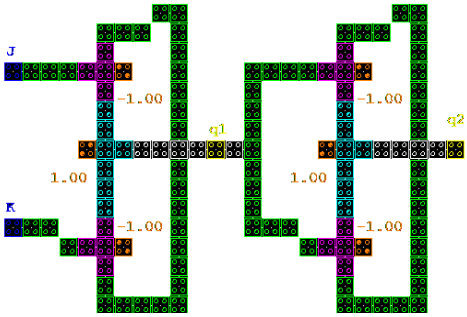


Fig 14 (a) QCA JK Flip flop

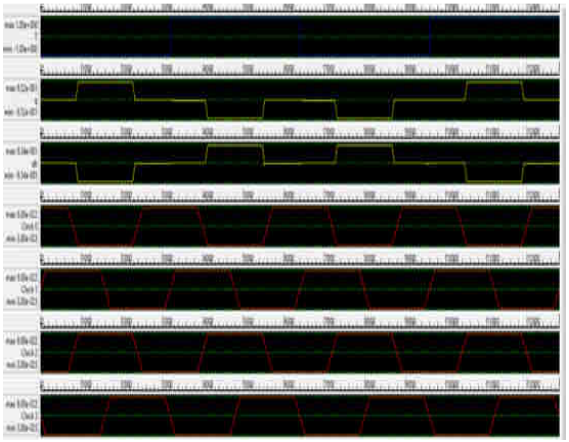


Fig. 14(b)Simulation result of JK flip flop

Fig .15 shows the T flip flop circuit and its simulation result. T flip flop has a simpler function if compared to JK flip flop as its only uses one input in its design. T flip flop holds its previous output when the input entered is logic 0 and toggle its previous output when the input entered is logic 1.

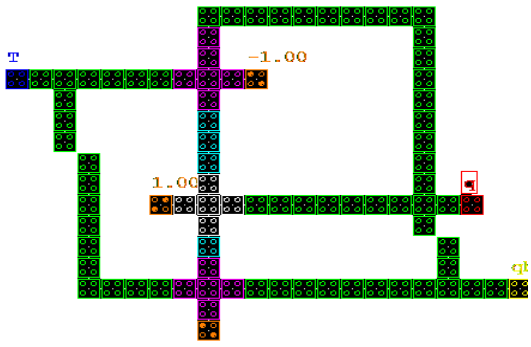


Fig. 15(a) T Flip flop

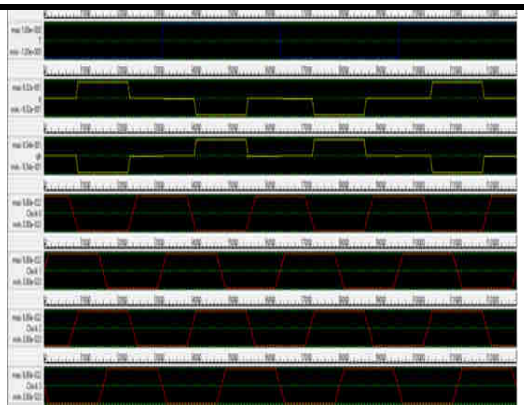


Fig.15(b) simulation result of T flip flop

ii) Counters and Shifters

The 2 bit synchronous up counter shown in figure 16 is built by cascading two T flip flops. A T flip flop is achieved by tying together the two inputs of JK flip flop. Output A gives the least significant bit of the 2 bit counter. T o produce the most significant bit ,output B has to be complemented every two cycles. when output A is logic 0,output B will hold, and when output A is logic 1,output B will toggle. I n short, output B is complemented when output A goes from logic 1 to logic 0. An n-bit counter can be produced by cascading more flip flops in series.

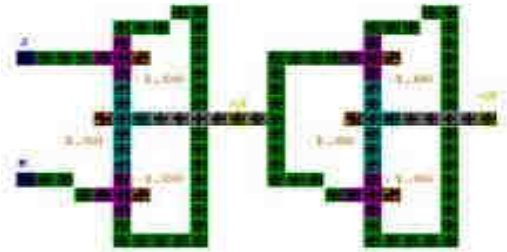


Fig.16(a) QCA 2-bit counter

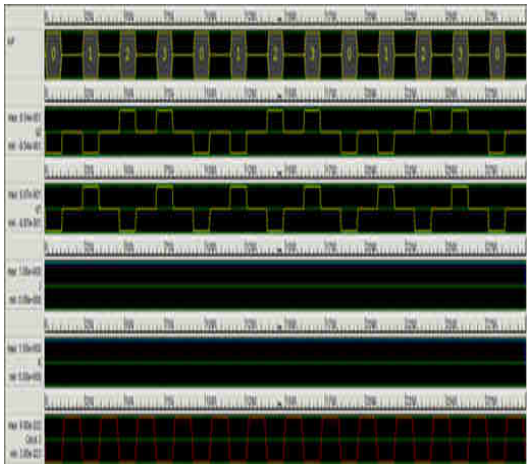


Fig.16(b) Simulation result of QCA 2 bit counter

A 4- bit shift register, as shown in fig 17 consists of a chain of four cascading flip flops, where the output of one flip flop is connected to the input of the next flip flop. The shift register is unidirectional. The data is shifted one bit position to the right for each clock cycle.

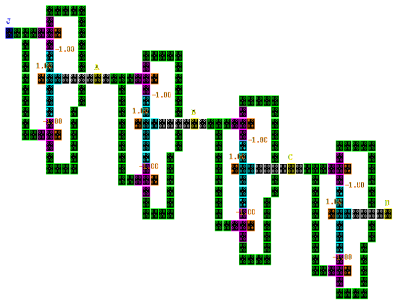


Fig.17(a) QCA 4 bit shift register

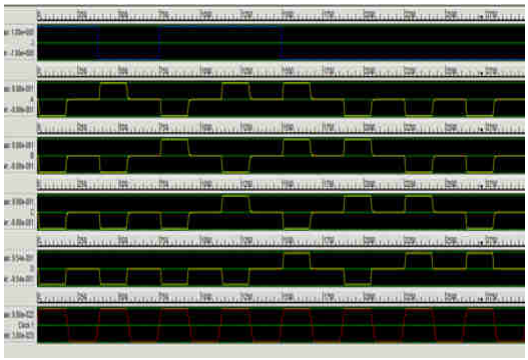


Fig.17(b) Simulation result of QCA shift register

C .COUNTERS AND REGISTERS

The total size of each circuit is tabulated in Table 2.As the designs become more complicated, more QCA cells are required. To overcome this, crossover technique might be used to reduce the device size. The size of circuit can also be reduced by optimizing the use of majority gate.

Table 1.Latches and flip flops-Size and No. of QCA cells

Name of circuit	Total size of circuit	Number of cells
D flip flop	0.01 μm^2	73
RS-latch (active high)	0.06 μm^2	37
RS-latch (active low)	0.06 μm^2	37
Gated D-latch	0.12 μm^2	81
JK flip-flop	0.12 μm^2	80
T flip-flop	0.16 μm^2	86
D flip-flop	0.20 μm^2	104
2-Bit counter	0.16 μm^2	118
4 bit shift register	0.50 μm^2	234

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