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Nat Nanotechnol. Author manuscript; available in PMC 2010 September 1.

Published in final edited form as:

Nat Nanotechnol. 2010 March ; 5(3): 190–194. doi:10.1038/nnano.2010.8.

## **Graphene nanomesh**

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## Abstract

Graphene has significant potential for application in electronics<sup>1-5</sup>, but cannot be used for effective field-effect transistors operating at room temperature because it is a semimetal with a zero bandgap<sup>6,7</sup>. Processing graphene sheets into nanoribbons with widths of less than 10nm can open up a bandgap that is large enough for room temperature transistor operation<sup>8-19</sup>, but nanoribbon devices often have low driving currents or transconductances<sup>18,19</sup>. Moreover, practical devices and circuits will require the production of dense arrays of ordered nanoribbons, which is of significant challenge<sup>20,21</sup>. Here we report the production of a new graphene nanostructure which we call graphene nanomesh - that can open up a band gap in a large sheet of graphene to create a semiconducting thin film. The nanomeshes are prepared with block copolymer lithography and can have variable periodicities and neck widths down to 5 nm. Graphene nanomesh field-effect transistors can support currents nearly 100 times greater than individual graphene nanoribbon devices, and the on-off ratio - which is comparable with the values achieved in individual nanoribbon devices - can be tuned by varying the neck width. The block copolymer lithography approach used to make the nanomesh devices is intrinsically scalable and could allow for the rational design and fabrication of graphene-based devices and circuits with standard semiconductor processing.

The Graphene nanomesh (GNM) reported here is a single or few-layer of graphene with a high density array of nanoscale holes punched in (Fig. 1g). For the convenience of discussion, we define two critical structural parameters in a GNM: the "periodicity" defined as the center-to-center distance between two neighboring nanoholes, and the "neck width" defined as the smallest edge-to-edge distance between two neighboring nanoholes in the nanomesh.

Figure 1 illustrates our approach to fabricate GNMs. For initial demonstrations, we use mechanically peeled graphene flakes as the starting material, although the approach described here can be readily extended to graphene films obtained through chemical exfoliation or chemical vapour deposition<sup>22-25</sup>. A 10-nm thick silicon oxide (SiO<sub>x</sub>) film is first evaporated onto graphene as the protecting layer and also the grafting substrate for the

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Author Contributions X.D, Y.H. and J.B. conceived and designed the experiments. J.B. X.Z. S.J. performed the experiments. J.B. collected and analyzed the data. J.B., Y.H. and X.D. wrote the paper. All authors discussed the results and commented on the manuscript.

following block copolymer nanopatterning<sup>26</sup>. The poly(styrene-block-methyl methacrylate) (P(S-b-MMA)) block copolymer thin film with cylindrical domains normal to the surface is then fabricated and used as the etching template<sup>26</sup>, and a CHF<sub>3</sub> based reactive ion etch (RIE) process followed by oxygen plasma etch is employed to punch holes into the graphene layer (see Methods for details).

Atomic force microscopy (AFM) image of the annealed P(S-b-MMA) thin film shows the cylindrical PMMA domains packed hexagonally within the PS matrix (Fig. 2a). The domain center-to-center distance is approximately 39 nm by using P(S-b-MMA) with a molecular weight of 77,000 g mol<sup>-1</sup> and a PS:PMMA volume ratio of 70:30. Changing the molecular weight while keeping the volume ratio constant can result in vertical aligned domains with variable center-to-center distance (Supplementary Fig. S1)<sup>27</sup>. After UV exposure and glacial acid development to remove PMMA domains, a porous structure of PS matrix with hexagonally arranged nanoholes vertically penetrating through the film is obtained (Fig. 2b). The following etching process drills into the underneath SiO<sub>x</sub> layer, leaving a SiO<sub>x</sub> nanomesh that can serve as the mask for subsequent oxygen plasma etch to form GNMs (Fig. 2c). The oxide mask can be easily removed by briefly dipping the sample into HF solution and the GNM structure can be seen under SEM (Fig. 2d).

To unambiguously determine the GNM structure, we have carried out extensive transmission electron microscopy (TEM) studies (see Methods for details). Fig. 3a-h shows a series of TEM images of the GNMs with variable periodicities or neck widths. For better image contrast, most TEM images are taken from GNMs with a relative large thickness (5-10 nm), although images of GNMs with one or a-few-layer graphene have also been obtained but typically with lower contrast (Supplementary Fig. S2). TEM studies clearly shows GNM structure with nearly hexagonally arranged nanoholes, consistent with SEM studies. Figures 3a and e show TEM images of a GNM obtained from copolymer mask with molecular weight of 77000 g mol<sup>-1</sup>, with a nanohole periodicity of ca. 39 nm, and average neck width of 14.6 nm. The nanoholes observed here are slightly larger than the PMMA domains in the self-assembled block copolymer pattern due to slight over etch in the fabrication process. Importantly, such nanomesh structure can be readily seen over many microns and apparently is only limited by the size of starting graphene fakes (Supplementary Fig. S3).

Our fabrication process shows great versatility in controlling both the neck width and the periodicity independently. For example, the neck width can be tuned through controlled over etching during the fabrication process. Figures 3b and f show the TEM images of a nanomesh with the same periodicity of ca. 39 nm, but smaller average neck with of 11.2 nm through controlled lateral over etch of PS mask. Figures 3c and g show a nanomesh with average neck width of 7.1 nm obtained with additional over etch. Furthermore, it is also possible to tune the mesh periodicity and neck width by using block copolymer of different molecular weight<sup>27</sup>. Figures 3d and h show a much denser GNM with smaller periodicity of ca. 27 nm and average neck width of 9.3 nm obtained using smaller molecular weight block copolymer thin film as the mask template.

As the GNM neck width represents the smallest dimension that controls charge transport through the system, we have carried out statistical analysis of the neck widths of the GNMs obtained with variable etching conditions or different block copolymer masks (Fig. 3i-1). The histograms resulted from the statistic analysis show that a series of GNMs with variable neck widths of 14.6, 11.2, 7.1 and 9.3 nm have been achieved. The standard deviation of the GNM neck width is in general less than 2 nm. The smallest neck width we observed to date is about 5 nm through even more aggressive over etching (Supplementary Fig. S4). In this deep nanometer regime, this aggressive over-etch may lead to the breakage of some necks in

the nanomesh due to a finite standard deviation, and the yield can be limited. However, we note our block copolymer assembly process is not yet optimized to the best it can offer, and the optimization of the block copolymer self-assembly<sup>28,29</sup> can lead to more uniform nanomesh that afford more aggressive over etch for even smaller neck width. These TEM studies clearly demonstrate that highly uniform GNMs can be obtained with controllable periodicities and neck widths using the block copolymer nanolithography.

This ability to control the nanomesh periodicity and neck width is very important for controlling their electronic properties because charge transport properties is highly dependent on the width of the critical current pathway. In the case of graphene nanoribbons (GNRs), both theoretical and experimental works have shown that the size of the conduction band gap is inversely proportional to the ribbon width<sup>8-19</sup>. The GNMs can be viewed as a highly interconnected network of GNRs. Therefore, narrow neck width is needed to gain enough bandgap for sufficient gate response and on-off ratio, and denser mesh structure can enable higher current delivery.

To investigate the electronic properties of the GNMs, we have fabricated GNM based transistors and carried out electrical transport studies. A three terminal device is fabricated using the GNM as the semiconducting channel, e-beam evaporated Ti/Au pads as the source-drain contacts, a highly doped p-type silicon substrate as the back gate and a 300-nm thermal oxide as the gate dielectric (Fig. 4a, b). Figures 4c and d show the electrical transport characteristics of a typical GNM transistor with estimated neck width of ca. 10 nm. Drain current ( $I_d$ ) versus drain-source voltage ( $V_d$ ) relations at various gate voltages ( $V_o$ ) for the GNM transistor show typical p-channel transistor behaviour (Fig. 4c). The hole-doping observed in the GNM is similar to GNR devices, and can be attributed to edge oxidation in the O2 plasma process or physisorbed oxygen from the ambient and other species during the sample preparation steps. The plots of  $I_d$  versus  $V_g$  (Fig. 4d) at a constant  $V_d = -10$  mV, -100 mV and -500 mV show little current when the V<sub>g</sub> is more positive than a threshold voltage ( $V_{th}$ ) of -0.6 V, and I<sub>d</sub> increases nearly linearly when the V<sub>g</sub> increases in the negative direction. The plot shows the device has an on-state conductance as high as  $550 \,\mu\text{S}$ at  $V_g$ = -10 V, which is comparable to an array of ~50-100 parallel GNR devices<sup>18,19</sup>. The  $I_d$ - $V_g$  plots also show the device has an on-off ratio greater than 10, which is comparable to GNR FETs with width in the range of 10-15 nm<sup>18,19</sup>. Importantly, the on-off ratio of the GNM devices can be readily tuned by varying neck width. Additional studies show smaller on-off ratio of 6 for GNM device with larger neck width (~15 nm), and higher on-off ratio of more than 100 for GNM device with smaller neck width (~7 nm) (Fig. 4e and Supplementary Fig. S5). This observation is consistent with GNR devices where the conduction band gap and on-off ratio is inversely proportional to the width of the critical current pathway. Similar to GNRs, the opening of the conduction band gap in our GNM structure can be attributed to a combination of multiple factors including lateral quantum confinement<sup>8-10</sup> and localization effect resulted from edge disorder such as variable edge roughness or absorbed species in oxygen plasma etching process<sup>11,12</sup>. Elucidation of the exact origin of the band gap and investigation of the impact of exact edge termination will be an interesting topic in future studies. We believe the on-off ratio can be further increased upon additional shrinking the GNM neck width. These studies clearly demonstrate the formation of GNMs can effectively enable a semiconductor thin film with neck-width tunable electronic properties.

It is important to compare the performance of the GNM devices with that of bulk graphene or GNRs. The on-state conductivity for the 10-nm and 7-nm GNM device is approximately 1-2 orders of magnitude lower than that of bulk graphene<sup>5</sup>, but comparable to that of similar width GNRs<sup>18,19</sup>, although the total drive current can be 50-100 times greater than the GNR devices given the larger device width of the GNM device. The on-off ratio for our GNM

device is comparable to that of similar width  $GNRs^{18,19}$  with the highest on-off ratio observed in our 7-nm graphene nanomesh about 5-6 times larger than the largest on-off ratios reported in bulk graphene<sup>5</sup>. It should be noted that it is usually much more challenging to obtain a high on-off ratio (e.g. >100) than a medium on/off ratio (e.g. ~10) in a GNM device while maintaining a high on-state conductivity, since the high on-off ratio devices require to reduce the neck width by aggressive over etch that can lead to partial breakage of the GNM current pathway. It is also important to recognize that the requirement to achieve a similar on-off ratio in a bigger GNM device is much more stringent than in a smaller single GNR device, as each conducting channel need to be small enough to afford a large on-off ratio. The ability to achieve high on-off ratio and high current in our large GNM devices clearly highlights the relative uniformity of the current GNM film.

In conclusion, we have demonstrated a new graphene nanostructure — graphene nanomesh — that can effectively open up a conduction band gap in a large piece of graphene to form a continuous semiconducting thin film. We have shown that GNMs with variable periodicities and neck widths down to 5 nm can be prepared using block copolymer lithography. Using such nanomesh as semiconducting channel, we have demonstrated room temperature transistors with driving current nearly 100 times larger than those of individual GNR device, whilst with a comparable on-off ratio that is tunable by varying the neck widths. The block copolymer lithography fabrication of GNMs is an intrinsically scalable approach, and can therefore enable a continuous semiconducting GNM thin film that can be processed using standard semiconductor processing to fabricate integrated devices/circuits with designed characteristics to meet specific circuit requirements. The availability of such GNMs in deep nanometer regime will also provide an interesting system for fundamental investigation of transport behaviour in the highly interconnected graphene network and open exciting opportunities in highly sensitive biosensors and a new generation of spintronics<sup>30</sup>.

### METHODS

#### Preparation of block copolymer template

Graphene thin film was obtained by mechanically peeling of natural graphite onto silicon substrate with 300-nm thermal oxide. A 10-nm SiO<sub>x</sub> thin film was evaporated onto graphene using e-beam evaporator operated at  $10^{-6}$  torr. This fresh oxide surface was functionalized with P(S-r-MMA) random copolymer (Polymer Source, Mn: 11000, Mw/Mn: 1.15, styrene 55 mol%, functionalized  $\alpha$ -hydroxyl and  $\omega$ -tempo moiety) by spin coating a thin film from 1 wt% toluene solution. This film was annealed at 170 °C for 72 hours to anchor the polymer onto oxide surface through end hydroxyl group, and then rinsed with toluene to remove unanchored polymer. P(S-b-MMA) with molecular weight of 77000 g mol<sup>-1</sup> (PS-PMMA: 55000-22000, Mw/Mn: 1.09) and 47700 g mol<sup>-1</sup> (PS-PMMA: 35500-12200, Mw/Mn: 1.04) were purchased from Polymer Source and dissolved in toluene. The block copolymer thin film was prepared on the neutralized surface by spin coating 1 wt% filtered polymer solution at 2500 rpm followed by annealing at 180 °C for 12 hours. The thickness was determined to be 30-35 nm by AFM profile. Annealed film was exposed to 295-nm UV irradiation for 30 min under vacuum. The degraded PMMA domains were removed by immersing in glacial acid for 20 min followed by extensive water rinsing.

#### Formation of graphene nanomesh

We used reactive ion etcher (STS MESC Multiplex Advanced Oxide Etcher) to etch down to graphene layer. Firstly, an O<sub>2</sub> plasma process (50 W, 4 mTorr) was used to remove exposed random copolymer. Controlled over etching here can be used to enlarge the nanoholes in PS nanomesh. Then,  $CHF_3$  plasma (50 W, 6 mTorr) was employed to punch holes into evaporated  $SiO_x$  to expose underlying graphene layer. Additional O<sub>2</sub> plasma was

used to completely etch away exposed region of graphene or to further undercut the graphene nanomesh.

#### **Microscopic characterizations**

TEM samples were prepared by spin coating 300 nm thick of PMMA polymer resist onto the graphene mesh substrate and baked at 100 °C. The PMMA-graphene mesh film was then lifted off in HF solution and transferred onto the lacey film coated copper grid. After PMMA was removed by acetone vapour, the sample was characterized by JEOL 1200 operated at 80kV. Tapping mode AFM was done with a Veeco 5000. SEM imaging was performed on a JEOL 6700F operated at 5 kV.

#### **Supplementary Material**

Refer to Web version on PubMed Central for supplementary material.

#### Acknowledgments

We acknowledge Electron Imaging Center for Nanomachines (EICN) at UCLA for the technical support of TEM, Nanoelectronics Research Facility at UCAL for technical support of device fabrication. We thank R. Kaner and D. Neuhauser for discussions, J. Chen and C. Liu for assistance in statistics analysis, F. X. Xiu for assistance in block copolymer processing. Y.H. acknowledges support from the Henry Samueli School of Engineering and an Applied Science Fellowship. X.D. acknowledges partial support by the NIH Director's New Innovator Award Program, part of the NIH Roadmap for Medical Research, through grant number 1DP2OD004342-01.

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#### Figure 1. Schematic of making graphene nanomesh

**a**, A pristine graphene flake on top of silicon oxide substrate as starting material. **b**, The graphene flake is covered by a thin layer of evaporated  $SiO_x$  and a thin film of spin coated block copolymer poly(styrene-block-methyl methacrylate) (P(S-b-MMA)). The  $SiO_x$  here is used as protecting layer and the grafting substrate for the following block copolymer nanopatterning. **c**, The P(S-b-MMA) block copolymer film is annealed and developed, leaving the porous PS matrix as nanomesh template for further patterning. **d**, Fluoride based reactive ion etching (RIE) to penetrate oxide layer and partially degrade PS film, and form  $SiO_x$  nanomesh hard mask. **e**, Graphene in the exposed area is etched away by  $O_2$  plasma. **f**, After HF dip to remove oxide mask, a GNM is obtained. **g**, Free standing GNM can be lifted off from the substrate by etching away underlying silicon oxide.





**a**, An AFM phase contrast image of the annealed block copolymer film on graphene shows hexagonal packed PMMA domains in the PS matrix. **b**, An SEM image of a porous PS film obtained by selectively removing the PMMA domains. **c**, An SEM image of the SiO<sub>x</sub> nanomesh mask after reactive ion etching with PS mask. **d**, An SEM image of a GNM structure after removing top SiO<sub>x</sub> mesh mask. All scale bars indicate 100 nm.



#### Figure 3. TEM studies of graphene and thin layer graphite nanomesh

**a,e**, TEM images of GNMs with periodicity of 39 nm and neck width of 14.6 nm obtained with block copolymer P(S-b-MMA) of molecular weight of 77000 g mol<sup>-1</sup>. **b,f**, GNM with periodicity of 39 nm and neck width of 11.2 nm obtained with controlled over etching. **c,g**, GNM with periodicity of 39 nm and neck width of 7.1 nm obtained with additional over etching. **d,h**, GNM with periodicity of 27 nm and neck width of 9.3 nm obtained with block copolymer P(S-b-MMA) of smaller molecular weight of 47700 g mol<sup>-1</sup>. The dark strips in the background of the images originate from the lacey carbon on TEM grids. Scale bars for (**a-d**) indicate 200 nm and scale bars for (**e-h**) indicate 100 nm. **i-l**, Histograms of the GNM neck width for (**e-h**) with average neck widths of 14.6 nm, 11.2 nm, 7.1 nm and 9.3 nm; and standard deviations of 2.0 nm, 1.9 nm, 1.5 nm and 1.3 nm, respectively.



#### Figure 4. Room temperature electrical properties of graphene nanomesh device

**a**, A schematic of a GNM-FET. The device is fabricated on heavily doped silicon substrate with 300-nm SiO<sub>2</sub> as the gate dielectric. The electronic measurement was done in ambient at room temperature without removing top oxide layer. **b**, An SEM image of a GNM device made from nanomesh with a periodicity ca. 39 nm, and neck width of ca. 10 nm. Scale bar indicates 500 nm. **c**, Drain current (I<sub>d</sub>) versus drain-source voltage (V<sub>d</sub>) recorded at different gate voltage for a GNM device with channel width of ~ 2 µm and channel length of ~ 1 µm. The on state conductance at V<sub>g</sub>=-10 V is comparable to an array of 100 parallel GNR devices. **d**, Transfer characteristics for the device in (**c**) at V<sub>d</sub> = -10 mV, -100 mV and -500 mV. The ratio between I<sub>on</sub> to I<sub>off</sub> for this device is ~ 14 at V<sub>d</sub> = -100 mV. **e**, Transfer characteristics at V<sub>d</sub> = -100 mV for GNMs with different estimated neck widths of ~15 nm (device channel width 6.5 µm and length 3.6 µm), ~10 nm (channel width 2 µm and length 1 µm), and ~7 nm (channel width 3 µm and length 2.3 µm).